REMARKS

The Patent Office objects to the Drawing under 37 C.F.R. § 1.84(p)(5) as lacking reference characters listed in the specification. Due to the amendments to the specification, the objection to the missing reference characters is now moot.

Claims 1-19 have been examined on their merits.

Claim 19 has been withdrawn from consideration.

Applicants herein editorially amend claims 2-10 and 12-18 to conform the claims to U.S. practice. The amendments to claims 2-10 and 12-18 were not made for reasons of patentability.

Applicants thank the Patent Office for indicating that claims 2-10 and 13-18 would be allowed if rewritten in independent form. Instead of rewriting claims 2-10 and 13-18 in independent form, Applicants respectfully traverse the art-based rejections of claims 1, 11 and 12 for at least the reasons discussed below.

Claims 1-19 are all the claims presently pending in the application.

1. Claim 11 stands objected to as containing informalities. Applicants herein amend claims 8, 11 and 13 to remove the word "apt" from the claims. Applicants submit that the objection to claim 11 has been overcome, and respectfully request withdrawal of same.

2. Claims 1, 11 and 12 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Farwell (U.S. Patent No. 5,870,445). Applicants traverse the § 102(b) rejection of claims 1, 11 and 12 for at least the reasons discussed below.

Farwell is directed to a frequency independent clock synchronizer. As mentioned in Farwell, a clock system of a digital system generates clock signals and distributes such clock signals to multiple points of use to synchronize changes in the state of the digital system. The purpose of Farwell is to provide a phase compensation clock synchronizing circuit that uses only a single clock, allows for unlimited frequency range, and accommodates clock gating.
As shown in Fig. 1 of Farwell, the clock synchronizing circuit includes an input buffer 11 that receives a master reference clock signal RCLK and sends a clock signal to a clock distribution tree 19 via a variable delay circuit 13, an inverter 15, and a clock buffer 17. The clock distribution tree provides a plurality of in-phase distributed clock signals ECLK to a plurality of clocked digital devices 21. A feedback clock signal FCLK that is representative of the distributed clock signals ECLK is taken from the input of one of the clocked digital devices and provided to a feedback buffer 23. The output of the feedback buffer 23 and the output of the input buffer 11 are provided as inputs to a phase comparator 25, which adjusts the delay of the variable delay circuit 13 such that the feedback clock signal FCLK, which is representative of the distributed clock signals ECLK, is delayed by one clock pulse width relative to the reference clock RCLK.

Thus, in Farwell, the phase comparator 25 compares the buffered reference clock signal BCLK and a distributed clock signal ECLK. In other words, Farwell compares the phase of the

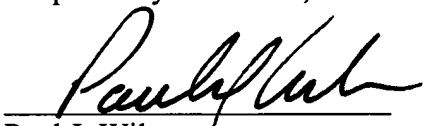
reference signal and the phase of the output of the clock distribution system. There is no teaching or suggestion in Farwell, however, of an input data flow comprising a sure data sequence and containing a logic transition. The Patent Office cites col. 1, lines 61-62 of Farwell as allegedly disclosing the sure data sequence containing a logic transition. All that the cited portion of Farwell discloses is providing a variable delay line, free of discontinuities, for a phase compensation clock synchronizing circuit. There is no teaching or suggestion in Farwell of an input data sequence having a sure data sequence containing a logic transition even interacts with such a circuit. The only input into Farwell is the master reference clock signal RCLK, and an input data sequence comprising a sure data sequence containing a logic transition is completely absent.

Based on at least the foregoing reasons, Applicants submit that claims 1 and 11 are allowable over Farwell, and further submit that claim 12 is allowable as well, at least by virtue of its dependency from claim 11. Applicants respectfully request that the Patent Office reconsider and withdraw the § 102(b) rejection of claims 1, 11 and 12.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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